

Appln No. 09/650,275
Amdt date August 31, 2004
Reply to Office action of July 8, 2004

REMARKS/ARGUMENTS

The above identified patent application has been amended. Entry of the Amendment and reconsideration and reexamination are hereby requested.

Claims 1 - 5, 7, 8, 14 - 22, 24 - 27 are now in the application. Claims 6, 9 - 13 and 23 have been cancelled. Claims 1, 14 and 18 have been amended.

The Examiner has objected to the Specification because of informalities.

The Applicant has amended the Specification to correct the informalities.

The Examiner has rejected Claims 1 - 8 and 14 - 27 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner indicates that there is no support in the specification for an elongate region being electrically isolated from the remainder of the substrate except at the gap.

The Examiner has similarly rejected Claims 1 - 8 and 14 - 27 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

The Applicant, however, submits that there is support in the specification and drawings for an elongate region being electrically isolated from the remainder of the substrate except at the gap and that the claims are not indefinite in that regard.

This is clearly set forth in the amended paragraph of the Specification set forth hereinabove, and in the Summary of the Invention, page 2, line 14 through page 3, line 18, where it states (underlining added for emphasis):

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"The present invention is directed to a seal structure and method for forming a seal structure for a semiconductor die. An elongate region that is electrically isolated from the remainder of the substrate, such as a well region of a conductivity type opposite that of the substrate, extends around the major portion of the periphery of the substrate. A gap is left between the two ends of the elongate region along the minor portion of the periphery of the substrate not covered by the elongate region. A conductive seal ring is formed around the periphery of the substrate at the elongate region and spans the gap between the ends of the elongate region. The substrate of the semiconductor die is only brought into electrical contact with the seal ring at the gap between the ends of the elongate region.

Allowing the substrate to electrically contact the seal ring only at a minor portion of the seal ring ensures that the short circuit between the seal ring and the substrate is limited to a small portion of the semiconductor die. Thus, the only low resistance electrical path between the substrate and the seal ring is confined to the small portion of the seal ring in electrical contact with the gap in the elongate region. With only one low resistance electrical path between the seal ring and the substrate, the seal ring no longer behaves as a conductive ring interconnecting all areas of the semiconductor die. The direct contact between the seal ring and the substrate at the gap is sufficient, however, to prevent the seal structure from accumulating charge while being manufactured. The location of the minor portion of the seal ring that contacts the substrate can be adjusted and optimized according to the specific circuit requirements. For example, in some applications it might be desirable to place the portion of the seal ring that contacts the substrate near the noisy area, or vice versa.

As mentioned above, the substrate and the well region of the preferred embodiment are formed having opposite conductivity types. The present invention allows for the substrate to have either a p-type or n-type conductivity, and the elongate region may be a well having either an n-type or p-type conductivity,

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respectively. Forming a well region with a conductivity opposite that of the substrate of the semiconductor die, and bringing the majority of the seal ring into physical contact only with the well region, reduces the ability of the semiconductor to communicate electrical signals, more specifically noise, through the seal ring to noise sensitive areas of the semiconductor die, without diminishing the protective benefits of the seal ring during manufacture of the die and during use of the semiconductor.

Other embodiments that isolate the seal ring from all or most of the substrate are also possible. For example, instead of the elongate well region, a high quality dielectric may be placed under the seal ring to electrically isolate it from the substrate. In another embodiment, the seal ring is electrically isolated from the substrate along the entire periphery of the die, and a separate low resistance path is provided between the seal ring and a power supply node to avoid a floating seal ring."

As such, and when read in conjunction with Fig. 3, it can be seen that elongate region 302 (which in one embodiment is an n-well) is electrically isolated from the remainder of the substrate (which is a P-substrate) except at the gap 304 (which is a P-substrate portion between the ends 322, 323 of n - well elongate region 302). As pointed out above "Forming a well region with a conductivity opposite that of the substrate of the semiconductor die, and bringing the majority of the seal ring into physical contact only with the well region, reduces the ability of the semiconductor to communicate electrical signals". In another embodiment, as also noted above the elongate region may be formed by "a high quality dielectric may be placed under the seal ring to electrically isolate it from the substrate." Accordingly, the Applicant submits that Claims 1 - 8 and 14

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- 27 comply with the written description requirement under 35 U.S.C. §112, first paragraph and are not indefinite under 35 U.S.C. §112, second paragraph.

The Examiner has rejected Claims 1 and 18 under 35 U.S.C. §102(b) as being anticipated by Joardar et al. The Examiner has also rejected under 35 U.S.C. §103(a): Claims 2 - 4, 6 - 7, 14 - 17, 19 - 21 and 23 - 24 as being unpatentable over Joardar et al. in view of Miyata; and Claims 5, 8, 22 and 25 - 27 as being unpatentable over Joardar et al. and Miyata and further in view of the Applicant's Admitted Prior Art.

The Applicant's amended Claims 1 and 14 now call for (underlining added for emphasis) ... a passive conductive seal ring extending around the entire periphery of the die within the elongate region and in direct contact with the substrate only at the gap. Relatedly, the Applicant's amended Claim 14 now calls for (underlining added for emphasis) ... a passive conductive seal ring extending around the entire periphery of the die within the elongate well region and in direct contact with the substrate only at the gap.

As such, the Applicant submits that independent Claims 1 and 18 are not anticipated by Joardar et al. under 35 U.S.C. §102(b) and that independent Claim 14 is not unpatentable under 35 U.S.C. §103(a) over Joardar et al. in view of Miyata

Joardar et al, while providing a circuit die having improved substrate noise isolation and includes a noise isolation ring, the noise isolation ring (107) is physically separated from the elongated ring (106). As such Joardar et al.s' seal ring does not extend around the entire periphery of the die within the elongate region and is not in direct contact with the substrate only at the gap.

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Accordingly, the Applicant submits that Claims 1 and 18 are not anticipated by Joardar et al. under 35 U.S.C. §102(b) and that Claim 14 is not unpatentable under 35 U.S.C. §103(a) over Joardar et al. in view of Miyata

Claims 2 - 5, 7 and 8 are dependent on Claim 1. Claims 15 - 17 are dependent on Claim 14. Claims 19 - 22, 24 - 27 are dependent on Claim 18. As such, these claims are believed allowable based upon Claims 1, 14 and 18 respectively.

Accordingly, in view of the above amendment and remarks it is submitted that the claims are patentably distinct over the prior art and that all the rejections to the claims have been overcome. Entry of this Amendment and reconsideration and reexamination of the above Application is requested.

Respectfully submitted,

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